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EXAMINER	
YIGDALL, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2122	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,857	KOH ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's response and replacement drawing sheets filed on November 1, 2004 have been fully considered. Claims 13-25 remain pending.

2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is noted, and the finality of that action is withdrawn. This Office action attempts to clarify the rejection set forth in the last action, the finality of which was necessitated by Applicant's amendment filed on May 20, 2004. Accordingly, this action is made final.

Response to Arguments

3. Applicant suggests that the Office action refers to descriptions of two embodiments of the invention taught by Sagane (Applicant's remarks, page 10). Applicant refers to column 6, lines 3-6 of Sagane and acknowledges, with regard to FIGS. 1 and 3 of Sagane, that "like reference characters designate like or corresponding parts" (Applicant's remarks, page 11). It should be noted that the same portion of Sagane further shows that "repetitive descriptions of the parts in FIG. 3 are omitted" (Sagane, column 6, lines 3-6). In other words, elements common to both the first and second embodiments (FIGS. 1 and 3, respectively) are not repeated in the description of the second embodiment.

Therefore, it is necessary to consider the description of the first embodiment when features common to both embodiments are not repeated in the description of the second embodiment. The portions of Sagane referred to in the rejection of claim 13 correspond to the second embodiment; the portions that happen to be found under the heading of the first embodiment are nonetheless pertinent to the second embodiment.

Specifically, and in response to Applicant's allegation that the Office action is vague at best (Applicant's remarks, page 8), FIG. 3 of Sagane illustrates a correction address register 21, which is a bug address setting register, and a comparator 8, which is a coincidence detecting circuit. Sagane expressly discloses a plurality of "comparators 8" and a plurality of "correction address registers 21" (column 6, line 67 to column 7, line 3). A correction address is the starting address of a buggy part of the program (column 3, lines 32-34). The definition of "correction address" does not change between the first and second embodiments.

Sagane further discloses that the comparator 8 compares an execution address with a correction address and outputs a coincidence signal when the addresses coincide (column 3, lines 48-52). Although the signal is labeled "E" in FIG. 1 and "A" in FIG. 3, the function and output of comparator 8 is common to both embodiments (column 6, lines 34-37). Sagane further discloses executing the program from ROM when there is no coincidence (column 6, lines 37-40), and executing a correction program from RAM, which is a debugging program, when the addresses coincide (column 6, lines 41-52).

4. Applicant contends that the Office action fails to show where and how the CPU 2 of FIGS. 1 and 3 of Sagane is to receive a plurality of coincidence signals, and similarly contends that Hosotani fails to disclose, teach or suggest the output of OR circuit 14 being applied to CPU 1 (Applicant's remarks, pages 11-12).

However, the second embodiment of Sagane provides for a plurality of comparators or coincidence detecting circuits (column 6, line 67 to column 7, line 3). Every such comparator disclosed by Sagane outputs a coincidence signal (column 3, lines 48-52). It would have been

apparent to one of ordinary skill in the art that the plurality of comparators would output a corresponding plurality of coincidence signals.

Furthermore, Hosotani discloses a plurality of changing address registers, which are bug address setting registers, and a plurality of match circuits, which are coincidence detecting circuits (FIG. 2). Each match circuit outputs a signal representing the result of an address comparison, for the purpose of correcting a plurality of bugs in the program (column 4, lines 30-59). Thus, Hosotani expressly discloses a plurality of coincidence signals. It would have been obvious to one of ordinary skill in the art to supplement Sagane with the features taught by Hosotani, for example to correct a plurality of bugs in ROM without incurring the expense of rebuilding the ROM (Hosotani, column 1, lines 45-50).

In Hosotani, the plurality of coincidence signals is "applied" to CPU 1 of FIG. 2 in the sense that the coincidence signals apply the appropriate connections to the data bus of the CPU (column 6, lines 34-39). Likewise, the CPU 1 of FIG. 2 "receives" the plurality of coincidence signals in the sense that the CPU receives data in accordance with those coincidence signals (column 6, lines 1-19).

Moreover, Sagane further discloses that the coincidence signal may generate an interrupt to signal the CPU that the addresses coincide (column 5, lines 13-16). In this case, the interrupt is the coincidence signal per se (column 3, lines 59-61), and as illustrated in FIG. 1, the signal is clearly connected to CPU 2. The access switching unit 7 provides the interrupt for signaling coincidence (column 3, lines 53-65). It would have been obvious to one of ordinary skill in the art to modify the second embodiment of Sagane such that access switching unit 7 of FIG. 1 substitutes for switch 23 of FIG. 3. The access switching unit 7 and the switch 23 are analogous

means by which control is switched between the program in ROM and the correction program in RAM (column 5, lines 8-21, and column 6, lines 41-52, respectively).

Therefore, Sagane discloses a plurality of coincidence detecting circuits, and suggests to one of ordinary skill in the art a corresponding plurality of coincidence signals. Sagane further discloses that the central processing unit may receive the coincidence signals as interrupts. Hosotani likewise discloses a plurality of coincidence detecting circuits, and expressly discloses the plurality of coincidence signals. Hosotani further suggests that the coincidence signals are applied to the central processing unit, as presented above.

Drawings

5. The objection to the drawings is withdrawn in view of the replacement drawing sheets filed on November 1, 2004 to remedy Figures 1 and 2 in a manner consistent with MPEP § 608.02(g).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 13-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,454,100 to Sagane (art of record) in view of U.S. Pat. No. 5,701,506 to Hosotani (art of record).

With respect to claim 13 (previously presented), Sagane discloses a data processing apparatus performing predetermined data processing in accordance with instruction codes read from a program memory storing a program (see, for example, column 1, lines 9-14), the data processing apparatus comprising:

(a) a debugging circuit having a plurality of bug address setting registers and a plurality of coincidence detecting circuits (see, for example, column 6, line 67 to column 7, line 3, which shows a plurality of correction address registers, i.e. bug address setting registers, and a plurality of comparators, i.e. coincidence detecting circuits),

(i) one of said plurality of bug address setting registers holding one of a plurality of bug addresses that show the start of a buggy part of said program stored in said program memory (see, for example, column 6, lines 7-9, which shows a bug address setting register holding a correction address, and column 3, lines 32-34, which shows that such a correction address denotes the start of a buggy part of the program),

(ii) one of said plurality of coincidence detecting circuits comparing a program address for reading instruction codes from said program memory with said one of said plurality of bug addresses held in said one of said plurality of bug address setting registers, said one of said plurality of coincidence detecting circuits outputting one of a plurality of coincidence signals when said program address and said one of said plurality of bug addresses coincide (see, for example, column 6, lines 34-37, which shows a coincidence detecting circuit comparing an execution address, i.e. a program address, with a bug address, and column 3, lines 48-52, which shows that such a coincidence detecting circuit outputs a coincidence signal when the addresses coincide),

(iii) another of said plurality of bug address setting registers holding another of said plurality of bug addresses that show the start of another buggy part of the program stored in the program memory (see, for example, column 6, lines 7-9, which shows a bug address setting register holding a correction address, i.e. another of the plurality of bug address setting registers holding another correction address, and column 3, lines 32-34, which shows that such a correction address denotes the start of a buggy part, i.e. another buggy part, of the program),

(iv) another of said plurality of coincidence detecting circuits comparing said program address for reading instruction codes from said program memory with said another of said plurality of bug addresses held in said another of said plurality of bug address setting registers, said another of said plurality of coincidence detecting circuits outputting another of said plurality of coincidence signals when said program address and said another of said plurality of bug addresses coincide (see, for example, column 6, lines 34-37, which shows a coincidence detecting circuit comparing an execution address with a bug address, i.e. another of the plurality of coincidence detecting circuits comparing a program address with a bug address, and column 3, lines 48-52, which shows that such a coincidence detecting circuit outputs a coincidence signal, i.e. another coincidence signal, when the addresses coincide); and

(b) a central processing unit (see, for example, CPU 2 in FIG. 3), wherein said central processing unit:

(i) executes one of a plurality of debugging programs stored within random access memory when said one of said plurality of coincidence signals indicates a coincidence of

said program address and said one of said plurality of bug addresses (see, for example, column 6, lines 41-52, which shows executing a correction program stored within RAM, i.e. a debugging program, when the addresses coincide),

(ii) executes another of said plurality of debugging programs stored within said random access memory when said another of said plurality of coincidence signals indicates a coincidence of said program address and said another of said plurality of bug addresses (see, for example, column 6, lines 41-52, which shows executing a correction program stored within RAM, i.e. another debugging program, when the addresses coincide), and

(iii) executes said program stored within said program memory when said plurality of coincidence signals indicates a non-coincidence of said program address and any of said plurality of bug addresses (see, for example, column 6, lines 37-40, which shows accessing ROM, i.e. executing the program stored within program memory, when there is no coincidence).

Although Sagane does not expressly disclose the limitation wherein the central processing unit receives a plurality of coincidence signals, the second embodiment of Sagane provides for a plurality of comparators or coincidence detecting circuits (see, for example, column 6, line 67 to column 7, line 3). Every such comparator disclosed by Sagane outputs a coincidence signal (see, for example, column 3, lines 48-52). It would have been apparent to one of ordinary skill in the art at the time the invention was made that the plurality of comparators would output a corresponding plurality of coincidence signals.

Furthermore, Hosotani discloses a plurality of changing address registers, i.e. bug address setting registers, and a plurality of match circuits, i.e. coincidence detecting circuits (see, for example, FIG. 2). Each match circuit outputs a signal representing the result of an address comparison, for the purpose of correcting a plurality of bugs in the program (see, for example, column 4, lines 30-59). Thus, Hosotani expressly discloses a plurality of coincidence signals. It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement Sagane with the features taught by Hosotani, for example to correct a plurality of bugs in ROM without incurring the expense of rebuilding the ROM (see, for example, Hosotani, column 1, lines 45-50).

In Hosotani, the plurality of coincidence signals is "applied" to CPU 1 of FIG. 2 in the sense that the coincidence signals apply the appropriate connections to the data bus of the CPU (see, for example, column 6, lines 34-39). Likewise, the CPU 1 of FIG. 2 "receives" the plurality of coincidence signals in the sense that the CPU receives data in accordance with those coincidence signals (see, for example, column 6, lines 1-19).

Moreover, Sagane further discloses that the coincidence signal may generate an interrupt to signal the CPU that the addresses coincide (see, for example, column 5, lines 13-16). In this case, the interrupt is the coincidence signal per se (see, for example, column 3, lines 59-61), and as illustrated in FIG. 1, the signal is clearly connected to CPU 2. The access switching unit 7 provides the interrupt for signaling coincidence (see, for example, column 3, lines 53-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second embodiment of Sagane such that access switching unit 7 of FIG. 1 substitutes for switch 23 of FIG. 3. The access switching unit 7 and the switch 23 are analogous means by

which control is switched between the program in ROM and the correction program in RAM (see, for example, column 5, lines 8-21, and column 6, lines 41-52).

Therefore, Sagane discloses a plurality of coincidence detecting circuits, and suggests to one of ordinary skill in the art a corresponding plurality of coincidence signals. Sagane further discloses that the central processing unit may receive the coincidence signals as interrupts. Hosotani likewise discloses a plurality of coincidence detecting circuits, and expressly discloses the plurality of coincidence signals. Hosotani further suggests that the coincidence signals are applied to the central processing unit, as presented above.

With respect to claim 14 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein an interrupt request for said central processing unit is generated when any of said plurality of coincidence signals indicates a coincidence of said program address and any of said plurality of bug addresses (see, for example, Sagane, column 5, lines 13-16, which shows generating an interrupt from the coincidence signal, i.e. any of the coincidence signals, when the corresponding addresses coincide).

Again, it would have been obvious to one of ordinary skill in the art to modify the second embodiment of Sagane such that access switching unit 7 of FIG. 1, which provides the interrupt for signaling coincidence (see, for example, column 3, lines 53-65), substitutes for switch 23 of FIG. 3. The access switching unit 7 and the switch 23 are analogous means by which control is switched between the program in ROM and the correction program in RAM (see, for example, column 5, lines 8-21, and column 6, lines 41-52).

With respect to claim 15 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein, when said one of said plurality of coincidence signals indicates said coincidence of said program address and said one of said plurality of bug addresses, said central processing unit:

(a) suspends execution of said program stored within said program memory after receiving said interrupt request (see, for example, Sagane, column 5, lines 11-20, which shows passing control to a correction program in RAM, i.e. suspending execution of the program in ROM, after receiving an interrupt request),

(b) processes an instruction stored within said random access memory at said one of said plurality of bug addresses to begin execution of said one of a plurality of debugging programs after suspending execution of said program (see, for example, Sagane, column 5, lines 17-21, which shows executing a correction program, i.e. a debugging program, at a correction address, i.e. a bug address, after suspending execution),

(c) suspends execution of said one of a plurality of debugging programs by processing an instruction residing within said one of a plurality of debugging programs that has a return address (see, for example, Sagane, column 5, lines 22-28, which shows returning to an address in ROM, i.e. suspending execution of a debugging program in RAM, by processing a jump instruction within the debugging program), and

(d) resumes execution of said program stored within said program memory by processing an instruction residing within said program memory at said return address (see, for example, Sagane, column 5, lines 25-31, which shows returning control to the program in ROM, i.e. resuming execution of the program at the return address).

With respect to claim 16 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein, when said another of said plurality of coincidence signals indicates said coincidence of said program address and said another of said plurality of bug addresses, said central processing unit:

(a) suspends execution of said program stored within said program memory after receiving said interrupt request (see, for example, Sagane, column 5, lines 11-20, which shows passing control to a correction program in RAM, i.e. suspending execution of the program in ROM, after receiving an interrupt request),

(b) processes an instruction stored within said random access memory at said another of said plurality of bug addresses to begin execution of said another of a plurality of debugging programs after suspending execution of said program (see, for example, Sagane, column 5, lines 17-21, which shows executing a correction program at a correction address, i.e. another of the plurality of debugging programs at another of the plurality of bug addresses, after suspending execution),

(c) suspends execution of said another of a plurality of debugging programs by processing an instruction residing within said another of a plurality of debugging programs that has a return address (see, for example, Sagane, column 5, lines 22-28, which shows returning to an address in ROM, i.e. suspending execution of another of the plurality of debugging programs in RAM, by processing a jump instruction within the debugging program), and

(d) resumes execution of said program stored within said program memory by processing an instruction residing within said program memory at said return address (see, for example,

Sagane, column 5, lines 25-31, which shows returning control to the program in ROM, i.e. resuming execution of the program at the return address).

With respect to claim 17 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein said plurality of bug addresses is stored within said random access memory (see, for example, Sagane, column 5, lines 44-48, which shows that the correction address, i.e. the bug address, is stored in RAM, and lines 49-54, which shows that there is a plurality of such bug addresses).

With respect to claim 18 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein said plurality of coincidence signals is a plurality of interrupt request signals (see, for example, Sagane, column 5, lines 13-16, which shows generating an interrupt request signal from the coincidence signal, and lines 49-54, which shows that there is a plurality of such interrupt request signals).

Again, it would have been obvious to one of ordinary skill in the art to modify the second embodiment of Sagane such that access switching unit 7 of FIG. 1, which provides the interrupt for signaling coincidence (see, for example, column 3, lines 53-65), substitutes for switch 23 of FIG. 3. The access switching unit 7 and the switch 23 are analogous means by which control is switched between the program in ROM and the correction program in RAM (see, for example, column 5, lines 8-21, and column 6, lines 41-52).

With respect to claim 19 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein said central processing unit receives said plurality of coincidence signals as separate interrupt requests (see, for example, Sagane, column 5, lines 13-16, which

shows generating an interrupt request signal from the coincidence signal, and lines 49-54, which shows repeating the interrupt sequence separately for each bug, i.e. such that the CPU receives the plurality of coincidence signals as separate interrupt requests).

Again, it would have been obvious to one of ordinary skill in the art to modify the second embodiment of Sagane such that access switching unit 7 of FIG. 1, which provides the interrupt for signaling coincidence (see, for example, column 3, lines 53-65), substitutes for switch 23 of FIG. 3. The access switching unit 7 and the switch 23 are analogous means by which control is switched between the program in ROM and the correction program in RAM (see, for example, column 5, lines 8-21, and column 6, lines 41-52).

With respect to claim 20 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein said central processing unit receives said plurality of coincidence signals as a single interrupt request (see, for example, Sagane, column 5, lines 13-16, which shows generating an interrupt request signal from the coincidence signal, and lines 49-54, which shows that there is a plurality of such interrupt request signals; further see, for example, Hosotani, column 4, line 60 to column 5, line 2, which shows that the plurality of coincidence signals becomes a single output signal).

Again, it would have been obvious to one of ordinary skill in the art to modify the second embodiment of Sagane such that access switching unit 7 of FIG. 1, which provides the interrupt for signaling coincidence (see, for example, column 3, lines 53-65), substitutes for switch 23 of FIG. 3. The access switching unit 7 and the switch 23 are analogous means by which control is switched between the program in ROM and the correction program in RAM (see, for example, column 5, lines 8-21, and column 6, lines 41-52).

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement Sagane with the features taught by Hosotani, for example to correct a plurality of bugs in ROM without incurring the expense of rebuilding the ROM (see, for example, Hosotani, column 1, lines 45-50).

With respect to claim 21 (previously presented), although Sagane in view of Hosotani discloses the limitation wherein said plurality of coincidence signals are input to said central processing unit as an interrupt request signal (see, for example, Sagane, column 5, lines 13-16, which shows generating an interrupt request signal from the coincidence signal, and lines 49-54, which shows that there is a plurality of such interrupt request signals), Sagane in view of Hosotani does not expressly disclose the limitation wherein said plurality of coincidence signals are logically AND'ed together.

However, Hosotani discloses that the coincidence signals are logically OR'ed together, and that the resulting output is at a "1" level when any one of the address comparisons is a match and at a "0" level when all of the comparisons are mismatches (see, for example, column 4, line 60 to column 5, line 2). In other words, Hosotani defines the coincidence detection circuitry as active high. When the signals are instead defined as active low, the same result is achieved by substituting the OR gate with an AND gate, as is well known in the art. The resulting output from the AND gate, in this case, would then be at a "0" level when any one of the address comparisons is a match and at a "1" level when all of the comparisons are mismatches.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the logical OR operation disclosed by Hosotani with a logical

AND operation when the coincidence detection circuitry is defined as active low, rather than active high as taught by Hosotani, to achieve an equivalent result.

With respect to claim 22 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein said plurality of debugging programs are input during initialization into said random access memory from a source external to said data processing apparatus (see, for example, Sagane, column 3, lines 32-46, which shows inputting the correction content, i.e. the plurality of debugging programs, into RAM from an external EEPROM during initialization).

With respect to claim 23 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein said random access memory stores a plurality of interrupt vectors of start addresses, said start addresses identifying memory areas within said random access memory that contain said plurality of debugging programs (see, for example, Sagane, column 5, lines 44-48, which shows that the start address is stored in RAM, and lines 49-54, which shows that there is a plurality of such start addresses that are interrupt vectors corresponding to the locations of a plurality of debugging programs in RAM).

With respect to claim 24 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein said central processing unit suspends an instruction being executed and reads an instruction code from a program address designated by a predetermined address table when said central processing unit executes any of said plurality of debugging programs stored within random access memory (see, for example, Sagane, column 6, lines 41-52, which shows reading instruction data from an address referenced by a predetermined address

table and executing a correction program stored within RAM, i.e. any of the plurality of debugging programs).

With respect to claim 25 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein said program memory is read only memory (see, for example, Sagane, column 1, lines 9-14, which shows that the program is stored in ROM).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (571) 272-3707. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

Michael J. Yigdall
Examiner
Art Unit 2122

mjy

WEI Y. ZHEN
PRIMARY EXAMINER